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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/431,076	11/01/1999	ICHIRO FUJIWARA	SON-1690	8227

7590 11/03/2003

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/431,076	Applicant(s) FUJIWARA, ICHIRO	
	Examiner Hung K. Vu	Art Unit 2811	

-- The MAILING DATE of this communication appears on th cov r sh t with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6-12 and 52-66* is/are pending in the application.

4a) Of the above claim(s) *3,5,52,62,63,65 and 66* is/are withdrawn from consideration.

5)☒ Claim(s) *54-56* is/are allowed.

6)☒ Claim(s) *1,2,4,9-12,53,57-61 and 64* is/are rejected.

7)☒ Claim(s) *6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1 A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant' submission filed on 08/19/03 has been entered. An action on the RCE follows.

Election/Restrictions

2. Newly submitted claims 62, 63, 65 and 66 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: they are not belong to elected embodiment of Figure 9.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 62, 63, 65 and 66 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4, 9-12, 53, 57-61 and 64 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujiwara et al. (PN 5,999,444, of record).

Fujiwara et al. discloses a nonvolatile semiconductor memory device comprising a plurality of memory elements (M11-M22) formed in the vicinity of the surface of a substrate (1), a plurality of word lines (WL1-WL2) for driving the memory elements, and a plurality of bit lines (BL1-BL2) [see Figures 1-2],

each of the plurality of memory elements including:

a semiconductor channel forming region (1a) formed in the vicinity of the surface of the substrate,

a source region (2) in contact with the channel forming region in the vicinity of the surface of the substrate,

a drain region (4) in contact with the channel forming region at a position facing the source region in the vicinity of the surface of the substrate,

a gate insulating film (6), including a tunnel insulating film (10,10a), formed on the substrate adjacent to the channel forming region,

a top insulating film (14) formed on the gate insulating film;

a conductive gate electrode (8) formed on the top insulating film on the gate insulating film, and

a charge storing means (12) facing the surface of the channel forming region and which is provided in the tunnel insulating film and in the gate insulating film and is planarly dispersed to the other neighbor charge storing means in the gate insulating film;

the gate electrode of the plurality of memory elements being respectively connected to the plurality of word lines [see Figure 2];

wherein the gate insulating film formed adjacent to the semiconductor channel forming region comprises a Fowler-Nordheim (FN) type tunneling film (10a) which has a FN type tunneling electroconductivity, the FN type tunneling film being made entirely of material having a dielectric constant greater than that of silicon oxide [oxynitride, see Col. 11, lines 45-48]. Note that the term "FN type tunneling" is method recitation in a device claimed. Also note that only the final product is relevant, not the method of making. A product by process claim is directed to the product per se, no matter how actually made. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

With regard to claim 2, Fujiwara et al. discloses the FN type tunneling film comprises any one of a nitride film, an oxynitride film, and aluminum oxide film, a tantalum pentaoxide film and a BST film, having an FN tunneling electroconductivity [see Col. 11, lines 45-48]. Note that the term "FN type tunneling" is method recitation in a device claimed. Also note that only the final product is relevant, not the method of making.

With regard to claim 4, Fujiwara et al. discloses the gate insulating film comprises a Pool-Frenkel (PF) type film including any one of a nitride film, an oxynitride film, and aluminum oxide film, a tantalum pentaoxide film and a BST film, having an FN tunneling electroconductivity [see Col. 11, lines 49-50]. Note that the term "PF type" is method recitation in a device claimed. Also note that only the final product is relevant, not the method of making.

With regard to claim 9, Fujiwara et al. discloses each memory transistor comprises the source region contacted to the channel forming region, and the drain region spaced to the source region and contacted to the channel forming region,

wherein a plurality of gate electrodes of the plurality of memory transistors are connected to a plurality of word lines [see Figure 2],

wherein the source region and drain region of each memory transistor are connected to a common line in a bit line direction, electrically insulated to and intersecting the word line, and

wherein the nonvolatile semiconductor memory device further comprises

a write inhibit voltage supply means (20) for supplying a reverse-biased voltage to the source region and/or the drain region of the memory transistor the gate electrode of which is connected to the word line selected at a writing, through the common line (SL2), to make the source region and/or the drain region in a reverse-biased state to the channel forming region, and

a non-selected word line biasing means (22) for supplying a voltage to a non-selected word line at the writing, a polarity of the voltage being a polarity making the non-selected word line in a reverse biased state to the channel forming region [see Figure 2 and Col. 4, lines 49-65].

With regard to claim 10, Fujiwara et al. discloses the write inhibit voltage supply means supplies the reverse bias voltage to the source region and/or the drain region to make a bias voltage of the memory transistor connected to the selected word line to thereby prevent an erroneous write and/or an erroneous erase [see Col. 3, line 11 – Col. 4, line 40].

With regard to claim 11, Fujiwara et al. discloses the non-selected word line biasing means supplies a voltage having a polarity for reverse-biasing to the non-selected word line to make a bias voltage or the memory transistor connected to the non-selected word line to thereby prevent an erroneous write and/or an erroneous erase [see Col. 3, line 11 – Col. 4, line 40].

With regard to claim 12, Fujiwara et al. discloses the non-selected word line biasing means biases the gate electrode to the source region so that a voltage of the gate electrode becomes a low level equal or lower than an inhibit gate voltage [see Figures 2 and 3].

With regard to claim 53, Fujiwara et al. discloses the gate insulating film (6) includes a tunnel insulating film (10,10a), a nitride film (12), and the top insulating film (14) in that order sandwiched between the surface of the substrate and the gate electrode, a portion of the gate insulating film overlapping each of the source region and the drain region [see Figure 1].

With regard to claim 57, Fujiwara et al. discloses when the reverse bias voltage is supplied to the channel forming region while the gate electrode and the channel forming region of the memory

transistor are dept at a same potential level, depletion layers extend from the source region and drain region to the channel forming region to merge them. [Col. 4, lines 27-40]

With regard to claim 58, Fujiwara et al. discloses the gate length of the memory transistor is shorter than a gate length given by, when the reverse bias voltage is supplied while the gate electrode and the channel forming region are dept at a same potential level, merged depletion layers extended from the source region and the drain region to the channel forming region. [Col. 4, lines 27-40]

With regard to claim 59, Fujiwara et al. discloses each memory transistor comprises:

a source region contacted to the channel forming region;

a drain region spaced to the source region and contact to the channel forming region;

wherein the nonvolatile semiconductor memory device comprises:

a source line commonly connecting the plurality of source regions of the plurality of memory transistors in the bit line direction;

a word line commonly connecting the plurality of gate electrodes of the plurality of memory transistors in a word direction. [Figure 2]

With regard to claim 60, Fujiwara et al. discloses each memory transistor comprises:

a source region contacted to the channel forming region;

a drain region spaced to the source region and contacted to the channel forming region;

wherein the nonvolatile semiconductor memory device comprises:

sub source lines commonly connecting the plurality of source regions of the plurality of memory transistors in a bit line direction;

a main source line commonly connecting the sub source lines in the bit line direction;

sub bit lines commonly connecting the plurality of drain regions of the plurality of memory transistors in the bit line direction;

a main bit line commonly connecting the sub bit line in the bit line direction;

a word line commonly connecting the plurality of gate electrodes of the plurality of memory transistors in a word direction;

a selected memory transistor being connected between the sub source line and the main source line and between the sub bit line and the man bit line. [Figure 2]

With regard to claim 61, Fujiwara et al. discloses the plurality of memory transistors are connected in series between the first selected transistor connected to a bit line and a second selected transistor connected to a common potential line. [Figure 2]

With regard to claim 64, Fujiwara et al. discloses the charge storing means does not have conductivity as a whole facing to the channel forming region when charges are not moved to the outside of the memory transistor. [Figure 1]

4. Claims 1, 2, 4 and 53 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura et al. (PN 6,518,617, of record).

Nakamura et al. discloses a nonvolatile semiconductor memory device comprising:

a semiconductor channel forming region (11a) formed in the vicinity of the surface of the substrate,

a source region in contact with the channel forming region in the vicinity of the surface of the substrate,

a drain region in contact with the channel forming region at a position facing the source region in the vicinity of the surface of the substrate,

a gate insulating film (12,13a,13b), including a tunnel insulating film (12), formed on the substrate adjacent to the channel forming region,

a top insulating film (13b) formed on the gate insulating film;

a conductive gate electrode (14) formed on the top insulating film on the gate insulating film, and

a charge storing means (13a) facing the surface of the channel forming region and which is provided in the tunnel insulating film and in the gate insulating film and is planarly dispersed to the other neighbor charge storing means in the gate insulating film;

wherein the gate insulating film formed adjacent to the semiconductor channel forming region comprises a Fowler-Nordheim (FN) type tunneling film (10a) which has a FN type tunneling electroconductivity, the FN type tunneling film being made entirely of material having a dielectric constant greater than that of silicon oxide [oxynitride, see Col. 4, lines 43-47, Col. 5, line 48-65].

It is inherent that nonvolatile memory device has a plurality of memory elements, a plurality of word lines, a plurality of bit lines and the gate electrode of the plurality of memory elements being connected to the plurality of word lines [see Fujiwara et al. (PN 5,999,444)].

Note that the term "FN type tunneling" is method recitation in a device claimed. Also note that only the final product is relevant, not the method of making. A product by process claim is directed to the product per se, no matter how actually made. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

With regard to claim 2, Nakamura et al. discloses the FN type tunneling film comprises any one of a nitride film, an oxynitride film, and aluminum oxide film, a tantalum pentaoxide film and a BST film, having an FN tunneling electroconductivity [see Col. 4, lines 43-47]. Note that the term "FN type tunneling" is method recitation in a device claimed. Also note that only the final product is relevant, not the method of making.

With regard to claim 4, Nakamura et al. discloses the gate insulating film comprises a Pool-Frenkel (PF) type film (13a) including any one of a nitride film, an oxynitride film, and aluminum oxide film, a tantalum pentaoxide film and a BST film, having an FN tunneling electroconductivity [see Col. 5, lines 49-57]. Note that the term "PF type" is method recitation in a device claimed. Also note that only the final product is relevant, not the method of making.

With regard to claim 53, Nakamura et al. discloses the gate insulating film includes a tunnel insulating film (12), a nitride film (13a), and the top insulating film (13b) in that order sandwiched between the surface of the substrate and the gate electrode, a portion of the gate insulating film overlapping each of the source region and the drain region [see Figure 1].

Allowable Subject Matter

5. Claims 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 54-56 are allowed.

7. The following is an examiner's statement of reasons for allowance:

Applicant's claims 6-8 and 54-56 are allowable over the references of record because none of these references disclose or can be combined to yield the claimed invention such as the pull-up electrode in the vicinity of the gate electrode or a wiring layer connected to the gate electrode, via a dielectric film, and a pull-up gate bias means for applying a voltage to the pull-up electrode.

Response to Arguments

8. Applicant's arguments filed 8/19/03 have been fully considered but they are not persuasive.

It is argued, at page 11 of the Remarks, that Fujiwara et al. fails to disclose a FN type tunneling film made entirely of material having a dielectric constant greater than that of silicon oxide since layer 10a represents only a portion of the tunnel insulating film. This argument is not convincing because Fujiwara et al. discloses a multiple tunneling films (10,10a) comprising the FN type

tunneling film 10a made entirely of material having a dielectric constant greater than that of silicon oxide. Since the claimed language does not clearly state whether there is only one tunneling film or the FN type tunneling film is in direct contact with the channel forming region, Applicant's claim 1 does not distinguish over the Fujiwara et al. reference.

It is argued, at page 12 of the Remarks, that Nakamura et al. fails to disclose a plurality of word lines, a plurality of bit lines and a gate electrode being respectively connected to the plurality of word lines since Nakamura et al. does not disclose the constitution and alignment of the word lines, bit lines and gate electrode connections, as described in the specification, to achieve various benefits over the prior art. This argument is not convincing because it is inherent that nonvolatile memory device has a plurality of memory elements, a plurality of word lines, a plurality of bit lines and the gate electrode of the plurality of memory elements being connected to the plurality of word lines. Further, it is noted that the features upon which applicant relies (i.e., the constitution and alignment of the word lines, bit lines and gate electrode connections to achieve various benefits over the prior art) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The

examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

October 24, 2003

Hung Vu

Patent Examiner